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Sterlite Technologies Limited
LETTER REPORT

SCOPE OF WORK

Testing of a cabling configuration Bit Error Rate (BER) and Frame Check Sequence (FCS) performance to the requirements of IEEE 802.3™ for 1000BASE-T operation.

REPORT NUMBER

105764505CRT-002

ISSUE DATE	**REVISED DATE**
18-March-2024	None
TESTS START DATE	**TESTS END DATE**
18-March-2024	18-March-2024

PAGES

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18-March-2024   Intertek Report No. 105764505CRT-002
Intertek Project No. G105764505

Mr. S.S. Harikanth
Sterlite Technologies Limited
33/1/1, Wagdhara Road
UT of Dadra and Nagerhaveli
Silvassa 396191
India

Subject: Bit Error Rate (BER) and Frame Check Sequence (FCS) errors testing of category 6 unshielded channel for support of 1000BASE-T operation

Dear Mr. Harikanth:

This letter report represents the results of our evaluation of the above referenced product(s) to the requirements contained in the following document(s):

IEEE Std 802.3^{TM}-2022 Standard for Ethernet, Approved 13-May-2012

SECTION 1
SUMMARY

Intertek wishes to inform you that the bit error rate and frame check sequence tests have been performed on your channel configuration. This testing was performed under project G105764505 and quotation CE-QUO-BAN-24-000478 issued 29-November-2023. Compliant results were obtained for the relevant tests contained in IEEE 802.3 for BER and FCS performance.

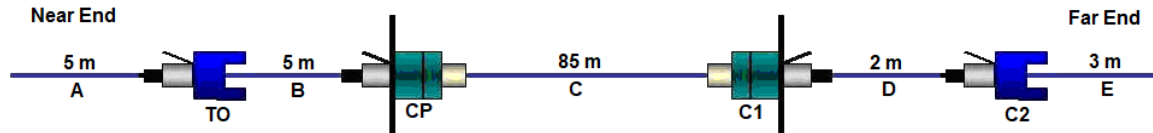## SECTION 2
NON-CONFORMANCES

None

SECTION 3
SAMPLE DESCRIPTION

The client supplied a 4-connector unshielded channel as illustrated below.

The samples were received on 12-March-2024 and were production samples in undamaged condition.

Component Id	Manufacturer	Description	Part number
A	Sterlite	U/UTP 24 AWG Patch Cord, 5M	NXPCC06UXZ24XX05
TO	Sterlite	Keystone jack, UTP, 90°	NXIOC06UX090XX
TO	Sterlite	Faceplate 2-Port	NXFP02BSXX
B	Sterlite	U/UTP 24 AWG Patch Cord, 5M	NXPCC06UXZ24XX05
CP	Sterlite	Keystone jack, UTP, 180°	NXIOC06UX180XX
CP	Sterlite	Patch Panel UTP 24 Port Unloaded	NXPPUX Series
C	Sterlite	U/UTP, LSZH Horizontal (solid) cable	2212X Series
C1	Sterlite	Keystone jack, UTP, 180°	NXIOC06UX180XX
C1	Sterlite	Patch Panel UTP 24 Port Unloaded	NXPPUX Series
D	Sterlite	U/UTP 24 AWG Patch Cord, 2M	NXPCC06UXZ24XX02
C2	Sterlite	Keystone jack, UTP, 90°	NXIOC06UX090XX
C2	Sterlite	Faceplate 1-Port	NXFP01BSXX
E	Sterlite	U/UTP 24 AWG Patch Cord, 3M	NXPCC06UXZ24XX03

SECTION 4
TEST EQUIPMENT USED

The following test equipment was used to conduct the testing.

Test equipment used	Model number	Control number	Calibration due date
Aukua Ethernet Monitoring Platform	MGA2510	0100439	Verify before use
Hioki Humidity/Temperature Sensor	Z2010	I084	16-January-2024

SECTION 5
TESTING

The following Ethernet events were monitored using the Aukua MGA2510 Ethernet monitoring platform.

Test description	Result
Bit Error Rate (BER)	No error measured
Frame Check Sequence (FCS) errors	No error measured
Link Loss Events	No loss of link
Errored LDCP Frames	No error measured

The screen capture is enclosed to this letter report.

SECTION 6
PROJECT STATUS & ACTION

Issuance of this letter report completes the performance testing of this channel cabling configuration BER and FCS performance per IEEE 802.3 covered by Intertek Project No. G105764505 and quotation CE-QUO-BAN-24-000478. The test results are compliant with the requirements of the standard and sections referred to on pages 2 and 4. The testing was performed at Intertek located in Cortland, NY.

If there are any questions regarding the results contained in this report, or any of the other services offered by Intertek, please do not hesitate to contact your dedicated Intertek Project Manager.

Completed by:	David Ayers		Reviewed by:	Antoine Pelletier
Title:	Technician		Title:	Project Engineer
Signature:			Signature	
Date	18-March-2024		Date:	18-March-2024

Please note: this Letter Report does not represent authorization for the use of any Intertek certification marks.

Port Configuration

| 1000BASE-T ▼ | Traffic Generator ▼ | Apply |

P1 RX P1 TX
98.70% 98.70%
P2 RX P2 TX
98.70% 98.70%

Capture Buffer
0B/2.0GB (0.0%)

TRIG IN ● TRIG OUT ● NTP ● CLK 10MHz ● CLK 1PPS ●

| Statistics | Generation | Filters | Capture | Jamming | Port Config | SMA Ports | Admin |

START ALL STOP ALL CLEAR ALARMS CLEAR STATS

| Stats Logging... | Pause | Graph: bottom ▼ |

Timestamp: 3:32:22 PM
Time Since Statistics Reset: 01:20:24
Traffic Routing for BER/Latency Test: P1→P2 / P2→P1

| Reset Rows | Select Rows... |

| Start P1 | Stop P1 | Start P2 | Stop P2 |

Port	Port 1	Port 2
Link	🟡	🟡
Port Bandwidth - Bits	986,996,160 RX|TX 986,996,016	986,996,160 RX|TX 986,996,016
Port Bandwidth - Packets	81,274 RX|TX 81,275	81,274 RX|TX 81,275
Port Bandwidth - Total Packets	391,823,797 RX|TX 391,823,798	391,823,797 RX|TX 391,823,798
Port Bandwidth - Line Utilization	1.0 Gbps RX|TX 1.0 Gbps	1.0 Gbps RX|TX 1.0 Gbps
Traffic Generator - Packets Generated	81,275	81,275
Traffic Generator - Total Packets Generated	391,823,797	391,823,797
Latency Measurement - Average	2.2122 µs	2.3123 µs
BER - Total Bit Errors Received	0	0
BER - Total Bit Error Rate	0e+0	0e+0
Error Stats - FCS Errors	0 RX|TX 0	0 RX|TX 0
Error Stats - Total FCS Errors	0 RX|TX 0	0 RX|TX 0
Error Stats - Receive LOS Count	-	-
Error Stats - Total Receive LOS Count	-	-
Error Stats - Total Errored LDPC Frames Received	-	-

| BER - Total Bit Error Rate ▼ | | Port 1: Bandwidth Received ▼ | | Port 2: Bandwidth Received ▼ |

■ Port 1 ■ Port 2

BER graph y-axis:
1.000e+0
9.000e-1
8.000e-1
7.000e-1
6.000e-1
5.000e-1
4.000e-1
3.000e-1
2.000e-1
1.000e-1
0.000e+0

x-axis: 15:31:00, 15:32:00

Port 1 Mbps — 987 (0 to 1,000)

Port 2 Mbps — 987 (0 to 1,000)

| Add another graph |

Computed Statistic Name:
Load

Computed Statistic:
((stats.inc_rx_pkts*20+stats.inc_rx_bytes)*8/1000).toFixed(0)

Computed Statistic Units:
kbps